



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,640	10/17/2003	Paul Stephen Andry	YOR20030192US1	8922
30678	7590	05/27/2005	EXAMINER	
CONNOLLY BOVE LODGE & HUTZ LLP SUITE 800 1990 M STREET NW WASHINGTON, DC 20036-3425			TRAN, MAI HUONG C	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/686,640

Applicant(s)

ANDRY ET AL.

Examiner

Mai-Huong Tran

Art Unit

2818

gm

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-44 is/are pending in the application.
- 4a) Of the above claim(s) 1-13 and 44 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 14-43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group II (Claims 14-43) drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 1-13 and 44 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14- are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S.

Patent No. 6,686,278 to Wang et al.

Regarding to claim 14, Wang discloses a method of fabricating a high aspect ratio, solid-metal filled via comprising providing a semiconductor substrate 400; defining a high aspect ratio via 420 in the substrate, wherein the via has a bottom and at least one sidewall; lining via bottom and at least one sidewall with a layer of an electrical insulator 410, wherein the insulator electrically isolates the via from the substrate; the lining insulator with a layer of an adhesion promoter 435; lining adhesion promoter 435 with a layer of a seed material 450; and filling via with a solid metal 470A (col. 5, lines 40-59, col. 6, lines 1-17, and figs. 4A-4F).

Regarding to claim 16, the method of fabricating a high aspect ratio, solid-metal filled via, wherein the via opens to a major surface of the semiconductor substrate (figs. 2-4).

Regarding to claim 17, the method of fabricating a high aspect ratio, solid-metal filled via, further comprising lining the major surface with a stack comprising a layer of an electrical insulator continuous with the insulator layer lining the via; a layer of an adhesion promoter continuous with the promoter layer lining the via; and a layer of a seed material continuous with the seed layer lining the via (col. 5, lines 40-59, col. 6, lines 1-17, and figs. 4A-4F).

Regarding to claim 18, the method of fabricating a high aspect ratio, solid-metal filled via, wherein the semiconductor substrate is selected from the group consisting of silicon, quartz, glass, and high temperature polymer (col. 1, line 28).

Regarding to claim 19, the method of fabricating a high aspect ratio, solid-metal filled via, wherein the insulator is selected from the group consisting of silicon nitride, silicon oxide, silicon oxynitride, and a SiN/SiO₂ stack (col. 5, lines 40-59).

Regarding to claim 20, the method of fabricating a high aspect ratio, solid-metal filled via, wherein the adhesion promoter is selected from the group consisting of Ta, Cr, Ti, TaN, and TiN (col. 5, lines 40-59).

Regarding to claim 21, the method of fabricating a high aspect ratio, solid-metal filled via, wherein the seed is selected from the group consisting of tungsten and molybdenum (col. 6, line 15).

Regarding to claim 22, the method of fabricating a high aspect ratio, solid-metal filled via, wherein the solid-metal filler is selected from the group consisting of tungsten, molybdenum, tantalum, and gold (col. 6, lines 14-17).

Regarding to claim 23, the method of fabricating a high aspect ratio, solid-metal filled via, wherein filling with a solid metal comprises a thermally-activated chemical vapor deposition (CVD) process (col. 5, lines 37-59).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,686,278 to Wang et al. in view of the remark.

Regarding to claim 15, Wand discloses the claimed invention except for the method of fabricating a high aspect ratio, solid-metal filled via wherein the aspect ratio of the via is from about 3:1 to about 10:1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the aspect ratio of the via is from about 3:1 to about 10:1, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims 24-43 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,686,278 to Wang et al. in view of Ziv et al. (5,060,595).

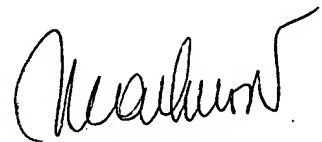
Regarding to claims 24-43, Wang discloses the claimed invention except for CVD comprises laser-assisted CVD (LCVD). However, Ziv teaches laser-assisted CVD (LCVD) (col. 5, line 10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use LCVD for the fabrication of a high aspect ratio, solid-metal filled via, as taught by Ziv in order to provide an apparatus and method for high rate deposition of small geometry metal vias of multilayer integrated circuit structures, especially those in which the depth to width aspect ratio of the vias is high, to provide a method and apparatus for filling via holes uniformly (col 3, lines 65-67, col. 4, lines 1-4).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mai-Huong Tran